**18ECC206J-VLSI DESIGN LAB**

# SEMESTER VI

## YEAR : 2022-2023

## NAME :

## REG NO :



**COLLEGE OF ENGINEERING AND TECHNOLOGY**

**DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING**

**SRM INSTITUTE OF SCIENCE AND TECHNOLOGY**

**(Under section 3 of UGC Act,1956)**

**SRM Nagar, Kattankulathur-603203**

**SRM INSTITUTE OF SCIENCE AND TECHNOLOGY COLLEGE OF ENGINEERING AND TECHNOLOGY**

**DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING**

**SRM Nagar,Kattankulathur-603203.**

**BONAFIDE CERTIFICATE**

# Register No:

Certified to be the bonafide record of work done by \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_of

\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ B.Tech Degree course in the Practical **18ECC206J-VLSI** **Design** in **SRM INSTITUTE OF SCIENCE AND TECHNOLOGY**, Kattankulathur during the Academic year **2022-2023 (Even Semester).**

**Date: Lab In-charge**

**Year Coordinator**

**Submitted for University Examination held in \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ in \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ SRM INSTITUTE OF SCIENCE AND TECHNOLOGY**, Kattankulathur

**Date: Examiner I Examiner II**

**Name : Class : III Year**

**Reg. No : Branch : ECE**

**INDEX**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **Experiment No** | **Date of Performance** | **Title of Experiment** | **Page No.** | **Date of Submission** | **Mark** | **Signature** |
|  |  |  |  |  |  |  |